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EXAMINER	
BROWN, MICHAEL J	
ART UNIT	**PAPER NUMBER**
2116	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/811,864	SINAI, DAVID	
	Examiner	Art Unit	
	Michael J. Brown	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/13/2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28,32,33,36,40,41,44,48,49 and 52-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28,32,33,36,40,41,44,48,49 and 52-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claims 28, 32-33, 36, 40-41, 44, 48-49, and 52-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takasaki et al.(US PGPub 2003/0140261) in view of Crouch et al.(US Patent 6,970,080) and further in view of Kouropoulos(US Patent 6,961,856).

As to claim 28, Takasaki discloses a method comprising providing an operating voltage(reference voltage sources 11 and 12, see Fig. 1) to a processor(CPU 3, see Fig. 1)(see paragraph 0024, lines 11-13 and paragraph 0027, lines 1-2), and modifying the operating voltage provided to the processor based on a mode of operation(low-rate clock; see paragraph 0024, line 13 and high-rate clock; see paragraph 0027, line 2) of the processor(see paragraph 0024, lines 11-13 and paragraph 0027, lines 1-2).

However Takasaki fails to specifically disclose the processor configured to process wireless signals, and sensing a level of power supplied to the processor in order to determine a current mode of operation.

Crouch teaches a processor(computer processor 12, see Fig. 4) configured to process wireless signals(see column 2, lines 32-34 and column 3, lines 16-17).

Kouropoulos teaches sensing a level of power supplied to a device(monitor; see column 2, line 10) in order to determine the current mode of operation(see column 2, lines 9-11). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply Crouch's processor which processes wireless signals to Takasaki's method of modifying the operational voltage of the processor based on the clock rate of the processor. It further would have been obvious to apply Kouropoulos' method of sensing of the power drawn by a monitor to Crouch's processor in order to determine its clock rate. The motivation to do so would be to selectively power down or power up the system upon reception of the wireless signal(see Crouch's Abstract, lines 10-13) ultimately based on a mode of operation of the processor.

As to claim 32, Takasaki discloses the method, wherein the operating voltage is modified by reducing the operating voltage when the current mode of operation is determined to be a sleep mode(see paragraph 0024, lines 11-13).

As to claim 33, Takasaki discloses the method, wherein the operating voltage is modified by increasing the operating voltage when the current mode of operation is determined to be an active mode(see paragraph 0027, lines 1-2).

As to claim 36, Takasaki discloses an apparatus comprising a power management controller(control circuit 1, see Fig. 1) to provide an operating voltage(reference voltage sources 11 and 12, see Fig. 1) to a processor(CPU 3, see Fig. 1)(see paragraph 0024, lines 11-13 and paragraph 0027, lines 1-2), and to modify the operating voltage based on a mode of operation(low-rate clock; see paragraph 0024, line 13 and high-rate clock; see paragraph 0027, line 2) of the processor(see paragraph 0024, lines 11-13 and paragraph 0027, lines 1-2). However, Takasaki fails to disclose the processor configured to process wireless communication signals, and Takasaki fails to disclose wherein the power management controller is configured to sense a level of power supplied to the processor in order to determine a current mode of operation.

Crouch teaches a processor(computer processor 12, see Fig. 4) configured to process wireless communication signals(see column 2, lines 32-34 and column 3, lines 16-17).

Kouropoulos teaches a power management controller configured to sense a level of power supplied to a device(monitor; see column 2, line 10) in order to determine the current mode of operation(see column 2, lines 9-11). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply Crouch's processor which processes wireless signals to Takasaki's method of modifying the operational voltage of the processor based on the clock rates of the processor. It further would have been obvious to apply Kouropoulos' method of sensing of the power drawn by a monitor to Crouch's processor in order to determine its clock rate. The

motivation to do so would be to selectively power down or power up the system upon reception of the wireless signal(see Crouch's Abstract, lines 10-13) ultimately based on a mode of operation of the processor.

As to claim 40, Takasaki discloses the apparatus, wherein the power management controller is able to modify the operating voltage by reducing the operating voltage when the current mode of operation is a sleep mode(see paragraph 0024, lines 11-13).

As to claim 41, Takasaki discloses the apparatus, wherein the power management controller is able to modify the operating voltage by increasing the operating voltage when the current mode of operation is an active mode(see paragraph 0027, lines 1-2).

As to claim 44, Takasaki discloses an article of manufacture comprising a storage medium(ROM 30 and EEPROM 31, see Fig. 4), and a set of instructions(program; see paragraph 0039, line 3) stored in the storage medium. Takasaki further discloses the set of instructions when executed by a power management controller(control circuit 1, see Fig. 1) cause the power management controller to perform operations comprising providing an operating voltage(reference voltage sources 11 and 12, see Fig. 1) to a processor(CPU 3, see Fig. 1)(see paragraph 0024, lines 11-13 and paragraph 0027, lines 1-2), and modifying the operating voltage provided to the processor based on a mode of operation(low-rate clock; see paragraph 0024, line 13 and high-rate clock; see paragraph 0027, line 2) of the processor(see paragraph 0024, lines 11-13 and paragraph 0027, lines 1-2). However Takasaki fails to

specifically disclose the power management controller configured to process wireless signals, and sensing a level of power supplied to the processor in order to determine a current mode of operation.

Crouch teaches a processor(computer processor 12, see Fig. 4) configured to process wireless signals(see column 2, lines 32-34 and column 3, lines 16-17).

Kouropoulos teaches sensing a level of power supplied to a device(monitor; see column 2, line 10) in order to determine the current mode of operation(see column 2, lines 9-11). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply Crouch's processor which processes wireless signals to Takasaki's method of modifying the operational voltage of the processor based on the clock rates of the processor. It further would have been obvious to apply Kouropoulos' method of sensing of the power drawn by a monitor to Crouch's processor in order to determine its clock rate. The motivation to do so would be to selectively power down or power up the system upon reception of the wireless signal(see Crouch's Abstract, lines 10-13) ultimately based on a mode of operation of the processor.

As to claim 48, Takasaki discloses the article of manufacture, wherein the operating voltage is modified by reducing the operating voltage when the current mode of operation is determined to be a sleep mode(see paragraph 0024, lines 11-13).

As to claim 49, Takasaki discloses the article of manufacture, wherein the operating voltage is modified by increasing the operating voltage when the current mode of operation is determined to be an active mode(see paragraph 0027, lines 1-2).

As to claim 52, Takasaki discloses a method comprising providing an operating voltage(reference voltage sources 11 and 12, see Fig. 1) to a processor(CPU 3, see Fig. 1)(see paragraph 0024, lines 11-13 and paragraph 0027, lines 1-2), and modifying the operating voltage provided to the processor based on a signal(low-rate clock; see paragraph 0024, line 13 and high-rate clock; see paragraph 0027, line 2). However Takasaki fails to specifically disclose the processor configured to process wireless signals, and receiving a signal indicating an anticipated mode of operation of the processor.

Crouch teaches a processor(computer processor 12, see Fig. 4) configured to process wireless signals(see column 2, lines 32-34 and column 3, lines 16-17).

Kouropoulos teaches receiving a signal indicating an anticipated mode of operation of a device(monitor; see column 2, line 10)(see column 2, lines 9-11). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply Crouch's processor which processes wireless signals to Takasaki's method of modifying the operational voltage of the processor based on the clock rates of the processor. It further would have been obvious to apply Kouropoulos' method of sensing of the power drawn by a monitor to Crouch's processor in order to determine its clock rate. The motivation to do so would be to selectively power down or power up the system upon reception of the wireless signal(see Crouch's Abstract, lines 10-13) ultimately based on a mode of operation of the processor.

As to claim 53, Takasaki discloses the method, wherein the operating voltage is modified by reducing the operating voltage in response to the signal when the anticipated mode of operation is a sleep mode(see paragraph 0024, lines 11-13).

As to claim 54, Takasaki discloses the method, wherein the operating voltage is modified by increasing the operating voltage when the anticipated mode of operation is an active mode(see paragraph 0027, lines 1-2).

As to claim 55, Takasaki discloses an apparatus comprising a power management controller(control circuit 1, see Fig. 1) to provide an operating voltage(reference voltage sources 11 and 12, see Fig. 1) to a processor(CPU 3, see Fig. 1)(see paragraph 0024, lines 11-13 and paragraph 0027, lines 1-2), and to modify the operating voltage based on a signal(low-rate clock; see paragraph 0024, line 13 and high-rate clock; see paragraph 0027, line 2) of the processor(see paragraph 0024, lines 11-13 and paragraph 0027, lines 1-2). However, Takasaki fails to disclose the processor configured to process wireless communication signals, and Takasaki fails to disclose wherein the power management controller is adapted to receive a signal indicating an anticipated mode of operation of the processor.

Crouch teaches a processor(computer processor 12, see Fig. 4) configured to process wireless communication signals(see column 2, lines 32-34 and column 3, lines 16-17).

Kouropoulos teaches a power management controller is adapted to receive a signal indicating an anticipated mode of operation of a device(monitor; see column 2, line 10)(see column 2, lines 9-11). It would have been obvious to one of ordinary skill in

the art at the time the invention was made to apply Crouch's processor which processes wireless signals to Takasaki's method of modifying the operational voltage of the processor based on the clock rates of the processor. It further would have been obvious to apply Kouropoulos' method of sensing of the power drawn by a monitor to Crouch's processor in order to determine its clock rate. The motivation to do so would be to selectively power down or power up the system upon reception of the wireless signal(see Crouch's Abstract, lines 10-13) ultimately based on a mode of operation of the processor.

As to claim 56, Takasaki discloses the apparatus, wherein the power management controller is able to modify the operating voltage by reducing the operating voltage in response to the signal when the anticipated mode of operation is a sleep mode(see paragraph 0024, lines 11-13).

As to claim 57, Takasaki discloses the apparatus, wherein the power management controller is able to modify the operating voltage by increasing the operating voltage in response to the signal when the anticipated mode of operation is an active mode(see paragraph 0027, lines 1-2).

As to claim 58, Takasaki discloses an article of manufacture comprising a storage medium(ROM 30 and EEPROM 31, see Fig. 4), and a set of instructions(program; see paragraph 0039, line 3) stored in the storage medium. Takasaki further discloses the set of instructions when executed by a power management controller(control circuit 1, see Fig. 1) cause the power management controller to perform operations comprising providing an operating voltage(reference

voltage sources 11 and 12, see Fig. 1) to a processor(CPU 3, see Fig. 1)(see paragraph 0024, lines 11-13 and paragraph 0027, lines 1-2), and modifying the operating voltage provided to the processor based a signal(low-rate clock; see paragraph 0024, line 13 and high-rate clock; see paragraph 0027, line 2). However Takasaki fails to specifically disclose the power management controller configured to process wireless signals, and receiving a signal indicating an anticipated mode of operation of the processor.

Crouch teaches a processor(computer processor 12, see Fig. 4) configured to process wireless signals(see column 2, lines 32-34 and column 3, lines 16-17).

Kouropoulos teaches receiving a signal indicating an anticipated mode of operation of a device(monitor; see column 2, line 10)(see column 2, lines 9-11). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply Crouch's processor which processes wireless signals to Takasaki's method of modifying the operational voltage of the processor based on the clock rate of the processor. It further would have been obvious to apply Kouropoulos' method of sensing of the power drawn by a monitor to Crouch's processor in order to determine its clock rate. The motivation to do so would be to selectively power down or power up the system upon reception of the wireless signal(see Crouch's Abstract, lines 10-13) ultimately based on a mode of operation of the processor.

As to claim 59, Takasaki discloses the article of manufacture, wherein the operating voltage is modified by reducing the operating voltage in response to the signal when the anticipated mode of operation is a sleep mode(see paragraph 0024, lines 11-13).

As to claim 60, Takasaki discloses the article of manufacture, wherein the operating voltage is modified by increasing the operating voltage in response to the signal when the anticipated mode of operation is an active mode(see paragraph 0027, lines 1-2).

Response to Arguments

2. Applicant's arguments, see Remarks, filed 11/13/2007, with respect to the rejection(s) of claim(s) 28, 32-33, 36, 40-41, 44, 48-49, and 52-60 under 35 U.S.C. 103(a) as being unpatentable over Yeh(US Patent 7,149,911) in view of Crouch et al.(US Patent 6,970,080) and further in view of Kouropoulos(US Patent 6,961,856) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Takasaki et al.(US PGPub 2003/0140261) in view of Crouch et al.(US Patent 6,970,080) and further in view of Kouropoulos(US Patent 6,961,856).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Brown whose telephone number is (571)272-5932. The examiner can normally be reached Monday-Thursday from 7:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571)272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Michael J. Brown
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REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
1/18/08